

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449</b>	Attorney Docket No. 2885/86	Serial No. 10/501,845
	Applicant(s) Vorbach et al.	
	Filing Date August 26, 2005	Group Art Unit 2183

**U.S. PATENT DOCUMENTS**

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	90/010,979	May 4, 2010 (filing date)	Vorbach et al.			
	90/011,087	July 8, 2010 (filing date)	Vorbach et al.			
	90/010,450	March 27, 2009 (filing date)	Vorbach et al.			
	5,212,777	May 18, 1993	Gove et al.			
	5,659,785	August 19, 1997	Pechanek et al.			
	6,173,419	January 9, 2001	Barnett			
	6,606,704	August 12, 2003	Adiletta et al.			
	6,668,237	December 23, 2003	Guccione et al.			
	6,836,842	December 28, 2004	Guccione et al.			
	2002/0010853	January 24, 2002	Trimberger et al.			
	2002/0152060	October 17, 2002	Tseng			

**FOREIGN PATENT DOCUMENTS**

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
	7-182167	July 21, 1995	Japan			Abstract	
	7-182160	July 21, 1995	Japan			Abstract	
	8-106443	April 23, 1996	Japan			Abstract	
	9-237284	September 9, 1997	Japan			Abstract	
	11-046187	February 16, 1999	Japan			Abstract	
	2001-236221	August 31, 2001	Japan			Abstract	
	2001-510650	July 31, 2001	Japan			Abstract	
	2002-0033457	January 31, 2002	Japan			Abstract	
	1044571	February 16, 1989	Japan			Abstract	

**OTHER DOCUMENTS**

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Altera, "2. TriMatrix Embedded Memory Blocks in Stratix & Stratix GX Devices," Altera Corporation, July 2005, 28 pages.
	Altera, "APEX II Programmable Logic Device Family," Altera Corporation Data Sheet, August 2002, Ver. 3.0, 99 pages.
	Ballagh et al., "Java Debug Hardware Models Using JBits," 8 <sup>th</sup> Reconfigurable Architectures Workshop, 2001, 8 pages.
	Becker, J., "A Partitioning Compiler for Computers with Xputer-based Accelerators," 1997, Kaiserslautern University, 326 pp.
	Bellows et al., "Designing Run-Time Reconfigurable Systems with JHDL," Journal of VLSI Signal Processing 28, Kluwer Academic Publishers, The Netherlands, 2001, pp. 29-45.
	"BlueGene/L - Hardware Architecture Overview," BlueGene/L design team, IBM Research, October 17, 2003 slide presentation, pp. 1-23.
	"BlueGene/L: the next generation of scalable supercomputer," Kissel et al., Lawrence Livermore National Laboratory, Livermore, California, November 18, 2002, 29 pages.
	BlueGene Project Update, January 2002, IBM slide presentation, 20 pages.

# INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449

Attorney Docket No.  
2885/86

Serial No.  
10/501,845

Applicant(s)  
Vorbach et al.

Filing Date  
August 26, 2005

Group Art Unit  
2183

EXAMINER'S  
INITIALS

AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.

BlueGene/L, "An Overview of the BlueGene/L Supercomputer," The BlueGene/L Team, IBM and Lawrence Livermore National Laboratory, 2002 IEEE, pp. 1-22.

Galanis, M.D. et al., "Accelerating Applications by Mapping Critical Kernels on Coarse-Grain Reconfigurable Hardware in Hybrid Systems," Proceedings of the 13<sup>th</sup> Annual IEEE Symposium on Field-Programmable Custom Computing Machines, 2005, 2 pages.

Guccione et al., "JBits: Java based interface for reconfigurable computing," Xilinx, Inc., San Jose, CA, 1999, 9 pages.

Guo, Z. et al., "A Compiler Intermediate Representation for Reconfigurable Fabrics," University of California, Riverside, Dept. of Electrical Engineering, IEEE 2006, 4 pages.

Gwennap, Linley, "P6 Underscores Intel's Lead," Microprocessor Report, Vol. 9., No. 2, February 16, 1995 (MicroDesign Resources), p. 1 and pp. 6-15.

Gwennap, Linley, "Intel's P6 Bus Designed for Multiprocessing," Microprocessor Report, Vol. 9, No. 7 (MicroDesign Resources), May 30, 1995, p.1 and pp. 6-10.

Hartenstein et al., "Parallelizing Compilation for a Novel Data-Parallel Architecture," 1995, PCAT-94, Parallel Computing: Technology and Practice, 13 pp.

Hartenstein et al., "A Two-Level Co-Design Framework for Xputer-based Data-driven Reconfigurable Accelerators," 1997, Proceedings of the Thirtieth Annual Hawaii International Conference on System Sciences, 10 pp.

Hauser, John Reid, (Dissertation) "Augmenting A Microprocessor with Reconfigurable Hardware," University of California, Berkeley, Fall 2000, 255 pages. (submitted in 3 PDFs, Parts 1-3)

Hauser, John R., "The Garp Architecture," University of California at Berkeley, Computer Science Division, October 1997, pp. 1-55.

Intel, "Pentium Pro Family Developer's Manual, Volume 3: Operating System Writer's Guide," Intel Corporation, December 1995, [submitted in 4 PDF files: Part I, Part II, Part III and Part IV], 458 pages.

Price et al., "Debug of Reconfigurable Systems," Xilinx, Inc., San Jose, CA, Proceedings of SPIE, 2000, pp. 181-187.

Sundararajan et al., "Testing FPGA Devices Using JBits," Proc. MAPLD 2001, Maryland, USA, Katz (ed.), NASA, CA, 8 pages.

Venkatachalam et al., "A highly flexible, distributed multiprocessor architecture for network processing," Computer Networks, The International Journal of Computer and Telecommunications Networking, Vol. 41, No. 5, April 5, 2003, pp. 563-568.

XILINX, "Virtex-II and Virtex-II Pro X FPGA User Guide," March 28, 2007, Xilinx user guide, pp. 1-559.

Xilinx, Inc.'s and Avnet, Inc.'s Disclosure Pursuant to P.R. 4-2; *PACT XPP TECHNOLOGIES, AG. V. XILINX, INC. and AVNET, INC.*, Case No. 2:07-cv-00563-TJW-CE, U.S. District Court for the Eastern District of Texas, Dec. 28, 2007, 4 pages.

Xilinx, Inc.'s and Avnet, Inc.'s Disclosure Pursuant to P.R. 4-1; *PACT XPP TECHNOLOGIES, AG. V. XILINX, INC. and AVNET, INC.*, Case No. 2:07-cv-00563-TJW-CE, U.S. District Court for the Eastern District of Texas, Dec. 28, 2007, 9 pages.

Defendant's Claim Construction Chart for P.R. 4-2 Constructions and Extrinsic Evidence for Terms Proposed by Defendants, *PACT XPP TECHNOLOGIES, AG. V. XILINX, INC. and AVNET, INC.*, Case No. 2:07-cv-00563-TJW-CE, U.S. District Court for the Eastern District of Texas, Dec. 28, 2007, pp. 1-19.

PACT's P.R. 4-1 List of Claim Terms for Construction, *PACT XPP TECHNOLOGIES, AG. V. XILINX, INC. and AVNET, INC.*, Case No. 2:07-cv-00563-TJW-CE, U.S. District Court for the Eastern District of Texas, Dec. 28, 2007, pp. 1-7.

PACT's P.R. 4-2 Preliminary Claim Constructions and Extrinsic Evidence, *PACT XPP TECHNOLOGIES, AG. V. XILINX, INC. and AVNET, INC.*, Case No. 2:07-cv-00563-TJW-CE, U.S. District Court for the Eastern District of Texas, Dec. 28, 2007, pp. 1-16, and EXHIBITS re EXTRINSIC EVIDENCE Parts in seven (7) separate additional PDF files (Parts 1-7).

EXAMINER

/Keith Vicary/

DATE CONSIDERED

09/22/2010

EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.